

WHAT IS CLAIMED IS:

- 1 1. A semiconductor device, comprising:
2 a workpiece including a first region and a second region;
3 a sensor formed in the first region;
4 at least one first insulating layer disposed over the sensor in the first region and disposed
5 over the second region;
6 a plurality of apertures formed in each at least one insulating layer over the sensor; and
7 a second insulating layer disposed over the at least one first insulating layer and the
8 plurality of apertures in the at least one first insulating layer, wherein each aperture forms a
9 hollow region beneath the second insulating layer within the at least one first insulating layer.
- 1 2. The semiconductor device according to Claim 1, further comprising interconnects formed
2 in the at least one first insulating layer in the second region of the workpiece.
- 1 3. The semiconductor device according to Claim 1, wherein the at least one first insulating
2 layer comprises a first thickness, wherein each aperture extends through the first thickness of the
3 at least one first insulating layer.
- 1 4. The semiconductor device according to Claim 3, wherein the at least one insulating layer
2 comprises a plurality of inter-metal dielectric (IMD) layers, the plurality of IMD layers
3 comprising a second thickness, wherein metal interconnects are formed within the plurality of
4 IMD layers, and wherein each aperture extends through the second thickness of the IMD layers.

1 5. The semiconductor device according to Claim 4, wherein the at least one insulating layer
2 comprises an inter-layer dielectric (ILD) layer disposed over and abutting the workpiece, the at
3 least one insulating layer comprising a third thickness, and wherein each aperture extends
4 through the third thickness of the ILD layer and the second thickness of the plurality of IMD
5 layers.

1 6. The semiconductor device according to Claim 5, wherein the ILD layer comprises about
2 4,000 Å to about 10,000 Å of SiO₂, fluorinated silicate glass (FSG) oxide, plasma-enhanced
3 oxide, high density plasma (HDP) oxide, or spin-on glass (SOG).

1 7. The semiconductor device according to Claim 5, further comprising a layer of silicon
2 nitride or silicon oxynitride disposed between the sensor and the ILD layer, the silicon nitride or
3 silicon oxynitride layer comprising a fourth thickness, wherein each aperture extends through the
4 fourth thickness of the silicon nitride or silicon oxynitride layer.

1 8. The semiconductor device according to Claim 5, further comprising a layer of silicon
2 nitride or silicon oxynitride disposed between the sensor and the ILD layer, the silicon nitride or
3 silicon oxynitride layer comprising a fourth thickness, wherein each aperture does not extend
4 through the fourth thickness of the silicon nitride or silicon oxynitride layer.

1 9. The semiconductor device according to Claim 4, wherein the plurality of IMD layers
2 comprise a plurality of layers comprising SiN, SiON, SiO₂, fluorinated silicate glass (FSG)
3 oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, spin-on glass (SOG), or
4 combinations thereof.

- 1 10. The semiconductor device according to Claim 4, wherein each IMD layer comprises a
2 barrier layer and an insulating layer disposed over the barrier layer.
- 1 11. The semiconductor device according to Claim 10, wherein each IMD layer insulating
2 layer comprises about 6,000 Å to about 11,000 Å of SiO₂, fluorinated silicate glass (FSG) oxide,
3 plasma-enhanced oxide, high density plasma (HDP) oxide, or spin-on glass (SOG), and wherein
4 each IMD layer barrier layer comprises about 100 Å to about 800 Å of SiN or SiON.
- 1 12. The semiconductor device according to Claim 1, wherein each aperture comprises a
2 shape of a circle, oval, square, rectangle, or a combination thereof.
- 1 13. The semiconductor device according to Claim 1, wherein each aperture comprises a
2 width of about 1.0 μm or less.
- 1 14. The semiconductor device according to Claim 1, wherein the plurality of apertures are
2 spaced apart by at least about 0.1 μm.
- 1 15. The semiconductor device according to Claim 1, wherein the second insulating layer
2 comprises a non-conformal dielectric material.
- 1 16. The semiconductor device according to Claim 1, wherein the second insulating layer
2 comprises a transparent or a translucent material.
- 1 17. The semiconductor device according to Claim 1, wherein the second insulating layer
2 comprises about 4000 Å to about 8000 Å of plasma enhanced (PE) oxide, silicon nitride (SiN)
3 or silicon oxynitride (SiON).

1 18. The semiconductor device according to Claim 1, wherein each aperture comprises a top
2 region, wherein the second insulating layer extends into the top region of each of the plurality of
3 apertures.

1 19. The semiconductor device according to Claim 1, wherein the sensor comprises a
2 photodiode.

- 1 20. A method of manufacturing a semiconductor device, the method comprising:
2 providing a workpiece, the workpiece including a first region and a second region;
3 forming a sensor in the first region;
4 forming at least one first insulating layer over the sensor in the first region and over the
5 second region;
6 forming a plurality of apertures in each at least one insulating layer over the sensor; and
7 forming a second insulating layer over the at least one first insulating layer and the
8 plurality of apertures in the at least one first insulating layer, wherein each aperture forms a
9 hollow region beneath the second insulating layer within the at least one first insulating layer.
- 1 21. The method according to Claim 20, further comprising forming interconnects in the at
2 least one first insulating layer in the second region of the workpiece.
- 1 22. The method according to Claim 20, wherein the at least one first insulating layer
2 comprises a first thickness, wherein forming the plurality of apertures comprises extending the
3 apertures through the first thickness of the at least one first insulating layer.
- 1 23. The method according to Claim 22, wherein forming the at least one insulating layer
2 comprises forming a plurality of inter-metal dielectric (IMD) layers, the plurality of IMD layers
3 comprising a second thickness, further comprising forming metal interconnects within the
4 plurality of IMD layers, and wherein forming the plurality of apertures comprises extending the
5 apertures through the second thickness of the IMD layers.

1 24. The method according to Claim 23, wherein forming the at least one insulating layer
2 comprises forming an inter-layer dielectric (ILD) layer disposed over and abutting the
3 workpiece, before forming the plurality of IMD layers, the at least one insulating layer
4 comprising a third thickness, and wherein forming the plurality of apertures comprises extending
5 the apertures through the third thickness of the ILD layer and the second thickness of the
6 plurality of IMD layers.

1 25. The method according to Claim 24, wherein forming the ILD layer comprises forming
2 about 4,000 Å to about 10,000 Å of SiO₂, fluorinated silicate glass (FSG) oxide, plasma-
3 enhanced oxide, high density plasma (HDP) oxide, or spin-on glass (SOG).

1 26. The method according to Claim 24, further comprising forming a layer of silicon nitride
2 or silicon oxynitride over the sensor, before forming the ILD layer, the silicon nitride or silicon
3 oxynitride layer comprising a fourth thickness, wherein forming the plurality of apertures
4 comprises extending the apertures through the fourth thickness of the silicon nitride or silicon
5 oxynitride layer.

1 27. The method according to Claim 24, further comprising forming a layer of silicon nitride
2 or silicon oxynitride over the sensor, before forming the ILD layer, the silicon nitride or silicon
3 oxynitride layer comprising a fourth thickness, wherein forming the plurality of apertures does
4 not comprise extending the apertures through the fourth thickness of the silicon nitride or silicon
5 oxynitride layer.

1 28. The method according to Claim 23, wherein forming the plurality of IMD layers
2 comprises forming a plurality of layers comprising SiN, SiON, SiO₂, fluorinated silicate glass
3 (FSG) oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, spin-on glass (SOG), or
4 combinations thereof.

1 29. The method according to Claim 23, wherein forming each IMD layer comprises forming
2 a barrier layer and forming an insulating layer over the barrier layer.

1 30. The method according to Claim 29, wherein forming each IMD layer insulating layer
2 comprises forming about 6,000 Å to about 11,000 Å of SiO₂, fluorinated silicate glass (FSG)
3 oxide, plasma-enhanced oxide, high density plasma (HDP) oxide, or spin-on glass (SOG), and
4 wherein forming each IMD layer barrier layer comprises forming about 100 Å to about 800 Å of
5 SiN or SiON.

1 31. The method according to Claim 20, wherein forming each aperture comprises forming a
2 shape of a circle, oval, square, rectangle, or a combination thereof.

1 32. The method according to Claim 20, wherein forming each aperture comprises forming an
2 aperture having a width of about 1.0 μm or less.

1 33. The method according to Claim 20, wherein forming the plurality of apertures comprises
2 forming the apertures spaced apart by at least about 0.1 μm.

1 34. The method according to Claim 20, wherein forming the second insulating layer
2 comprises forming a non-conformal dielectric material.

- 1 35. The method according to Claim 20, wherein forming the second insulating layer
2 comprises forming a transparent or a translucent material.
- 1 36. The method according to Claim 20, wherein forming the second insulating layer
2 comprises forming about 4000 Å to about 8000 Å of plasma enhanced (PE) oxide, silicon nitride
3 (SiN) or silicon oxynitride (SiON).
- 1 37. The method according to Claim 20, wherein each aperture comprises a top region,
2 wherein forming the second insulating layer comprises forming the second insulating layer in the
3 top region of each of the plurality of apertures.
- 1 38. The method according to Claim 20, wherein forming the sensor comprises forming a
2 photodiode.

1 39. A semiconductor device, comprising:
2 a workpiece including a first region and a second region;
3 a sensor formed in the first region;
4 at least one first insulating layer disposed over the sensor in the first region and disposed
5 over the second region, the at least one first insulating layer comprising a thickness;
6 interconnects disposed in the at least one first insulating layer in the second region of the
7 workpiece;
8 a plurality of apertures formed in each at least one insulating layer over the sensor in the
9 first region, each aperture extending through the thickness of the at least one first insulating
10 layer; and
11 a second insulating layer disposed over the at least one first insulating layer and the
12 plurality of apertures in the at least one first insulating layer, the second insulating layer
13 comprising a non-conformal dielectric material, wherein each aperture forms a hollow region
14 beneath the second insulating layer within the at least one first insulating layer.

1 40. The semiconductor device according to Claim 39, wherein the at least one first insulating
2 layer comprises SiN, SiON, SiO₂, fluorinated silicate glass (FSG) oxide, plasma-enhanced oxide,
3 high density plasma (HDP) oxide, spin-on glass (SOG), or combinations thereof, and wherein the
4 second insulating layer comprises plasma-enhanced oxide, SiN or SiON.

1 41. The semiconductor device according to Claim 39, wherein the second insulating layer
2 comprises a transparent or a translucent material.

1 42. The semiconductor device according to Claim 39, wherein each aperture comprises a top
2 region, wherein the second insulating layer extends into the top region of each of the plurality of
3 apertures.